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Patent Application

Inventor(s): C.W. Jones

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Title: METHOD AND APPARATUS FOR GENERATING AN OPTIMAL TEST PATTERN FOR SEQUENCE DETECTION

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5383143	01/1995	Crounch et al.			
	B	5144230	09/1992	Katoozi et al.			
	C	5258986	11/1993	Zerbe			
	D	5390192	02/1995	Fujieda			
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	F	5541942	07/1996	Strouss			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	G							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	H	Mississippi State University; EE3111 DIGITAL DEVICES DESIGN LABORATORY MANUAL, Fourth Edition; Jan. 1994
	I	Manoj Franklin and Kewal K. Saluja; EMBEDDED RAM TESTING; 1995 IEEE; pp.29-33
	J	H. Maeno, K. Nii, S. Sakayanagi and S. Kato; "LSSD COMPATIBLE AND CONCURRENTLY TESTABLE RAM;" 1992 International Test Conference Proceedings, IEEE; pp. 608-614
	K	H. Maeno, T. Hanibuchi, T. Tada, R. Walters, and T. Eto, "TESTING OF EMBEDDED RAM USING EXHAUSTIVE RANDOM SEQUENCES;" 1987 International Test Conference, IEEE; pp. 105-110

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.